Wafer-Level Integrated Systems:
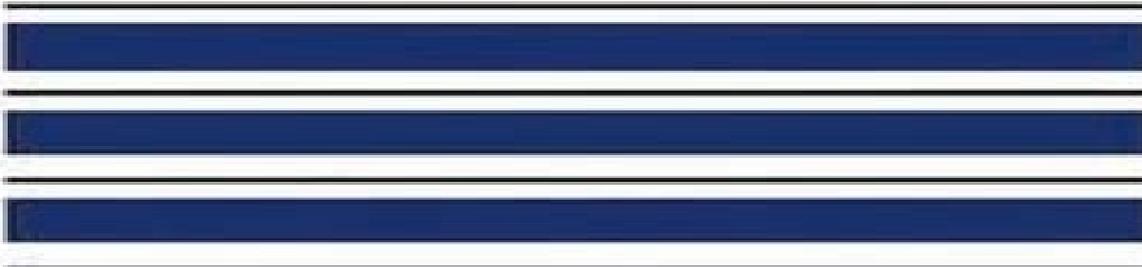## Implementation Issues

Stuart K. Tewksbury

Wafer Level Integrated Systems Implementation Issues

Stephen W. Director,Wojciech Maly,Andrzej J. Strojwas

Wafer Level Integrated Systems Implementation Issues:

Wafer-Level Integrated Systems Stuart K. Tewksbury,2012-12-06 From the perspective of complex systems conventional Ie s can be regarded as discrete devices interconnected according to system design objectives imposed at the circuit board level and higher levels in the system implementation hierarchy However silicon monolithic circuits have progressed to such complex functions that a transition from a philosophy of integrated circuits Ie s to one of integrated sys tems is necessary Wafer scale integration has played an important role over the past few years in highlighting the system level issues which will most significantly impact the implementation of complex monolithic systems and system components Rather than being a revolutionary approach wafer scale integration will evolve naturally from VLSI as defect avoidance fault tolerance and testing are introduced into VLSI circuits Successful introduction of defect avoidance for example relaxes limits imposed by yield and cost on Ie dimensions allowing the monolithic circuit s area to be chosen according to the natural partitioning of a system into individual functions rather than imposing area limits due to defect densities The term wafer level is perhaps more appropriate than wafer scale A wafer level monolithic system component may have dimensions ranging from conventional yield limited Ie dimensions to full wafer dimensions In this sense wafer scale merely represents the obvious upper practical limit imposed by wafer sizes on the area of monolithic circuits The transition to monolithic wafer level integrated systems will require a mapping of the full range of system design issues onto the design of monolithic circuit Defect and Fault Tolerance in VLSI Systems C.H. Stapper,V.K. Jain,Gabriele Saucier,2013-06-29 Higher circuit densities increasingly more complex application ohjectives and advanced packaging technologies have suhstantially increased the need to incorporate defect tolerance and fault tolerance in the design of VLSI and WSI systems The goals of defect tolerance and fault tolerance are yield enhancement and improved reliahility The emphasis on this area has resulted in a new field of interdisciplinary scientific research I n fact advanced methods of defect fault control and tolerance are resulting in enhanced manufacturahility and productivity of integrated circuit chips VI SI systems and wafer scale integrated circuits In 1987 Dr W Moore organized an International Workshop on Designing for Yield at Oxford University Edited papers of that workshop were published in reference II The participants in that workshop agreed that meetings of this type should he con tinued preferahly on a yearly hasis It was Dr I Koren who organized the IEEE Inter national Workshop on Defect and Fault Tolerance in VLSI Systems in Springfield Massachusetts the next year Selected papers from that workshop were puhlished as the first volume of this series 21 **Principles of VLSI System Planning** Allen M. Dewey,Stephen W. Director,2012-12-06 This book describes a new type of computer aided VLSI design tool called a VLSI System Planning that is meant to aid designers dur ing the early or conceptual state of design During this stage of design the objective is to define a general design plan or approach that is likely to result in an efficient implementation satisfying the initial specifications or to determine that the initial specifications are not realizable A design plan is a collection of high level design decisions As an example the

conceptual design of digital filters involves choosing the type of algorithm to implement e g finite impulse response or infinite impulse response the type of polyno mial approximation e g Equiripple or Chebyshev the fabrication technology e g CMOS or BiCMOS and so on Once a particu lar design plan is chosen the detailed design phase can begin It is during this phase that various synthesis simulation layout and test activities occur to refine the conceptual design gradually filling more detail until the design is finally realized The principal advantage of VLSI System Planning is that the increasingly expensive resources of the detailed design process are more efficiently managed Costly redesigns are minimized because the detailed design process is guided by a more credible consistent and correct design plan   Automatic Programming Applied to VLSI CAD Software: A Case Study Dorothy E. Setliff,Rob A. Rutenbar,2012-12-06 This book and the research it describes resulted from a simple observation we made sometime in 1986 Put simply we noticed that many VLSI design tools looked alike That is at least at the overall software architecture level the algorithms and data structures required to solve problem X looked much like those required to solve problem X Unfortunately this resemblance is often of little help in actually writing the software for problem X given the software for problem X In the VLSI CAD world technology changes rapidly enough that design software must continually strive to keep up And of course VLSI design software and engineering design software in general is often exquisitely sensitive to some aspects of the domain technology in which it operates Modest changes in functionality have an unfortunate tendency to require substantial and time consuming internal software modifications Now observing that large engineering software systems are technology dependent is not particularly clever However we believe that our approach to xiv Preface dealing with this problem took an interesting new direction We chose to investigate the extent to which automatic programming ideas cold be used to synthesize such software systems from high level specifications This book is one of the results of that effort   VLSI Design for Manufacturing: Yield Enhancement Stephen W. Director,Wojciech Maly,Andrzej J. Strojwas,2012-12-06 One of the keys to success in the IC industry is getting a new product to market in a timely fashion and being able to produce that product with sufficient yield to be profitable There are two ways to increase yield by improving the control of the manufacturing process and by designing the process and the circuits in such a way as to minimize the effect of the inherent variations of the process on performance The latter is typically referred to as design for manufacture or statistical design As device sizes continue to shrink the effects of the inherent fluctuations in the IC fabrication process will have an even more obvious effect on circuit performance And design for manufacture will increase in importance We have been working in the area of statistically based computer aided design for more than 13 years During the last decade we have been working with each other and individually with our students to develop methods and CAD tools that can be used to improve yield during the design and manufacturing phases of IC realization This effort has resulted in a large number of publications that have appeared in a variety of journals and conference proceedings Thus our motivation in writing this book is to put in one place a description of our approach to IC yield enhancement While the work that is

contained in this book has appeared in the open literature we have attempted to use a consistent notation throughout this book   **Mixed-Mode Simulation** Resve A. Saleh,A. Richard Newton,2012-12-06 Our purpose in writing this book was two fold First we wanted to compile a chronology of the research in the field of mixed mode simulation over the last ten to fifteen years A substantial amount of work was done during this period of time but most of it was published in archival form in Masters theses and Ph D dissertations Since the interest in mixed mode simulation is growing and a thorough review of the state of the art in the area was not readily available we thought it appropriate to publish the information in the form of a book Secondly we wanted to provide enough information to the reader so that a proto type mixed mode simulator could be developed using the algorithms in this book The SPLICE family of programs is based on the algorithms and techniques described in this book and so it can also serve as docu mentation for these programs ACKNOWLEDGEMENTS The authors would like to dedicate this book to Prof D O Peder son for inspiring this research work and for providing many years of support and encouragement The authors enjoyed many fruitful discus sions and collaborations with Jim Kleckner Young Kim Alberto Sangiovanni Vincentelli and Jacob White and we thank them for their contributions We also thank the countless others who participated in the research work and read early versions of this book Lillian Beck provided many useful suggestions to improve the manuscript Yun cheng Ju did the artwork for the illustrations   Computer Arithmetic Earl E Swartzlander,2015-03-17 This is the new edition of the classic book Computer Arithmetic in three volumes published originally in 1990 by IEEE Computer Society Press As in the original the book contains many classic papers treating advanced concepts in computer arithmetic which is very suitable as stand alone textbooks or complementary materials to textbooks on computer arithmetic for graduate students and research professionals interested in the field Told in the words of the initial developers this book conveys the excitement of the creators and the implementations provide insight into the details necessary to realize real chips This second volume presents topics on error tolerant arithmetic digit on line arithmetic number systems and now in this new edition a topic on implementations of arithmetic operations all wrapped with an updated overview and a new introduction for each chapter This volume is part of a 3 volume set Computer Arithmetic Volume I Computer Arithmetic Volume II Computer Arithmetic Volume III The full set is available for sale in a print only version Contents Error Tolerant ArithmeticOn Line ArithmeticVLSI Adder ImplementationsVLSI Multiplier ImplementationsFloating Point VLSI ChipsNumber RepresentationImplementations Readership Graduate students and research professionals interested in computer arithmetic Key Features It reprints the classic papersIt covers advanced arithmetic operationsIt does this in the words of the original creatorsKeywords Computer Arithmetic Fault Tolerant Arithmetic On Line Arithmetic Adder Implementations Multiplier Implementations Floating Point Chips Number Representation Implementations   **Wafer Scale Integration, III** Mariagiovanna Sami,Fausto Distante,1990 The purpose of this book is to give an up to date presentation of architectures and technologies for wafer scale integration As such it is an overview of the work of the leading research

centers active in this area and an outline of expected evolution and progress in the subject New technological solutions are envisioned while the use of optical technologies for interconnections promises to overcome one of the main restrictions to architectures on a wafer the extension of quick prototyping solutions to the wafer dimension allows the introduction of wafer scale systems in educational environments as well as in applications where a quick result and limited production would make traditional silicon solutions unacceptable Regarding architectures and their applications three different lines of approach can be identified Evolutive solutions are proposed mainly concerning array architectures and restructuring techniques Innovative architectures are presented several papers dealing with neural nets There are also architectures designed not just for experimental reasons but for industrial production Overall non numerical applications predominate **Gallium Arsenide Digital Circuits** Omar Wing,1990-10-31 Gallium Arsenide technology has come of age GaAs integrated circuits are available today as gate arrays with an operating speed in excess of one Gigabits per second Special purpose GaAs circuits are used in optical fiber digital communications systems for the purpose of regeneration multiplexing and switching of the optical signals As advances in fabrication and packaging techniques are made the operat ing speed will further increase and the cost of production will reach a point where large scale application of GaAs circuits will be economical in these and other systems where speed is paramount This book is written for students and engineers who wish to enter into this new field of electronics for the first time and who wish to embark on a serious study of the subject of GaAs circuit design No prior knowledge of GaAs technology is assumed though some previous experience with MOS circuit design will be helpful A good part of the book is devoted to circuit analysis to the extent that is possible for non linear circuits The circuit model of the GaAs transistor is derived from first principles and analytic formulas useful in predicting the approxi mate circuit performance are also derived Computer simulation is used throughout the book to show the expected performance and to study the effects of parameter variations **Handbook of VLSI Chip Design and Expert Systems** A. F. Schwarz,1993 Offers a conceptual and methodological understanding of chip design and of the fundamental principles in the computer aided design of VLSI circuits and systems CADCAS The text covers where why and how expert systems are used in subtasks of CADCAS and in the integrated chip design system **Proceedings, the IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems, November 13-15, 1995, Lafayette, Louisiana** IEEE Computer Society,1995 An invited talk recounts Intel s experience with increasing die yield through CAD algorithms and a panel discussion examines tools for the extracting of critical areas for a yield analysis of VLSI design Others of the 34 papers cover critical area analysis defect sensitivity and reliability fault tolerant architectures and arrays yield projection and enhancement fault tolerant and testing techniques and self checking and coding techniques No subject index Annotation copyright by Book News Inc Portland OR Hardware Design and Simulation in VAL/VHDL Larry M. Augustin,1991 The VHSIC Hardware Description Language VHDL provides a standard machine processable notation for describing hardware VHDL is the result of a collaborative effort between IBM

Intermetrics and Texas Instruments sponsored by the Very High Speed Integrated Cir cuits VHSIC program office of the Department of Defense beginning in 1981 Today it is an IEEE standard 1076 1987 and several simulators and other automated support tools for it are available commercially By providing a standard notation for describing hardware especially in the early stages of the hardware design process VHDL is expected to reduce both the time lag and the cost involved in building new systems and upgrading existing ones VHDL is the result of an evolutionary approach to language devel opment starting with high level hardware description languages existing in 1981 It has a decidedly programming language flavor resulting both from the orientation of hardware languages of that time and from a ma jor requirement that VHDL use Ada constructs wherever appropriate During the 1980 s there has been an increasing current of research into high level specification languages for systems particularly in the software area and new methods of utilizing specifications in systems de velopment This activity is worldwide and includes for example object oriented design various rigorous development methods mathematical verification and synthesis from high level specifications VAL VHDL Annotation Language is a simple further step in the evolution of hardware description languages in the direction of applying new methods that have developed since VHDL was designed **Hardware Annealing in Analog VLSI Neurocomputing** Bank W. Lee,Bing J. Sheu,1990-12-31 Rapid advances in neural sciences and VLSI design technologies have provided an excellent means to boost the computational capability and efficiency of data and signal processing tasks by several orders of magnitude With massively parallel processing capabilities artificial neural networks can be used to solve many engineering and scientific problems Due to the optimized data communication structure for artificial intelligence applications a neurocomputer is considered as the most promising sixth generation computing machine Typical applica tions of artificial neural networks include associative memory pattern classification early vision processing speech recognition image data compression and intelligent robot control VLSI neural circuits play an important role in exploring and exploiting the rich properties of artificial neural networks by using pro grammable synapses and gain adjustable neurons Basic building blocks of the analog VLSI neural networks consist of operational amplifiers as electronic neurons and synthesized resistors as electronic synapses The synapse weight information can be stored in the dynamically refreshed capacitors for medium term storage or in the floating gate of an EEPROM cell for long term storage The feedback path in the amplifier can continuously change the output neuron operation from the unity gain configuration to a high gain configuration The adjustability of the vol tage gain in the output neurons allows the implementation of hardware annealing in analog VLSI neural chips to find optimal solutions very efficiently Both supervised learning and unsupervised learning can be implemented by using the programmable neural chips **VLSI 91** Arne Halaas,Peter B. Denyer,1992 The major problem in VLSI is really the control of complexity The hardest part is the control of autonomous yet interacting processes We do not yet have satisfactory techniques for handling that sort of thing but I think the techniques we need to develop are independent of whether you are programming or designing the

chip Sidney Michaelson Initiator of the IFIP Working Group on VLSI This proceedings dedicated to the late Prof Sidney Michaelson who ten years ago established this IFIP Working Group reflects the continuing interest in improving design tools and the wide range of engineering concerns surrounding the effective exploitation of VLSI **Digital Optical Computing II** Raymond Arrathoon,1990 **Manufacturing Yield Evaluation of VLSI/WSI Systems** Bruno Ciciani,1995 A practical understanding of these concepts and their application can help to reduce the chance of having device failures **IEEE Proceedings of the Southeastcon** ,1990 Proceedings ,2003 *Proceedings of the 1991 International Symposium on Microelectronics, October 21-23, 1991, Orange County Convention Center, Orlando, Florida* ,1991 **Optical Interconnections and Networks** Hartmut Bartelt,1990

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